10/026,470.

COFC

Sterne Kessler Goldstein Fox
ATTORNEYS AT LAW

January 25, 2005

WRITER'S DIRECT NUMBER:
(202) 772-8629
INTERNET ADDRESS:
DONF@SKGF.COM

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Attn: Certificate of Correction Branch

Re: U.S. Issued Patent
Patent No. 6,828,654 B2; Issued: December 7, 2004
For: **Thick Oxide P-Gate NMOS Capacitor for Use in a Phase-Locked Loop Circuit and Method of Making Same**
Inventors: Tam *et al.*
Our Ref: 1875.1350000

Sir:

Transmitted herewith for appropriate action are the following documents:

1. Request for Certificate of Correction Under 37 C.F.R. § 1.322;
2. Copy of Amendment and Reply as filed on June 30, 2004;
3. Certificate of Correction Form (PTO/SB/44); and
4. One (1) return postcard.

It is respectfully requested that the attached postcard be stamped with the date of filing of these documents, and that it be returned to our courier. In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Donald J. Featherstone
Attorney for Patentees
Registration No. 33,876

DJF/LMY/lam
Enclosures

352242.1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent of:	Confirmation No.: 7771
Tam *et al.*	Art Unit: 2825
Patent. No.: 6,828,654 B2	Examiner: Malsawma, Lalrinfamkim H.
Issued: December 7, 2004	Atty. Docket: 1875.1350000
For: **Thick Oxide P-Gate NMOS Capacitor for Use in a Phase-Locked Loop Circuit and Method of Making Same**	

Request for Certificate of Correction Under 37 C.F.R. § 1.322

Attn: Certificate of Correction Branch

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

It is hereby requested that a Certificate of Correction under 37 C.F.R. § 1.322 be issued for the above-captioned United States Patent. This Certificate of Correction is being requested due to mistakes which appear in the printed patent. These mistakes were made by the U.S. Patent and Trademark Office.

Specifically, the printed patent contains the following errors for which a Certificate of Correction is respectfully requested:

In claim 1, column 6, line 55, "the said gate electrode and coupled to a second" should appear as --said gate electrode and coupled to a second--. Support for this correction can be found in the amendment to claim 6, as filed in the Amendment and Reply of June 30, 2004.

In claim 2, column 6, line 61, "The circuit of claim 1, wherein said P+ gate-to-substrate" should appear as --The circuit of claim 1, wherein the gate-to-substrate--. Support for this correction can be found in the amendment to claim 7, as filed in the Amendment and Reply of June 30, 2004.

In claim 6, column 7, line 5, "circuit additionally includes oscillator, a reference frequency" should appear as --circuit additionally includes an oscillator, a reference frequency--. Support for this correction can be found in the amendment to claim 11, as filed in the Amendment and Reply of June 30, 2004.

For convenience, a photocopy of the Amendment and Reply filed on June 30, 2004, is included herewith.

Remarks

The above-noted corrections do not involve such changes in the patent as would constitute new matter or would require reexamination.

A completed Form PTO/SB/44 accompanies this request, with the above-noted corrections printed thereon. Accordingly, a Certificate of Correction is believed proper and issuance thereof is respectfully requested.

The Commissioner is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Donald J. Featherstone
Attorney for Patentees
Registration No. 33,876

Date: 1/25/05

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

352219.1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:		Confirmation No.:	7771
	Tam *et al.*	Art Unit:	2825
Appl. No.:	10/026,470	Examiner:	Malsawma, L. H.
Filed:	December 27, 2001	Atty. Docket:	1875.1350000
For:	**A Thick Oxide P-Gate NMOS Capacitor for Use in a Phase-Locked Loop Circuit and Method of Making Same**		

Amendment and Reply Under 37 C.F.R. § 1.111

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reply to the Office Action dated March 1, 2004, (PTO Prosecution File Wrapper Paper No. 01292004), Applicants submit the following Amendment and Remarks. This Amendment is provided in the following format:

(A) Each section begins on a separate sheet;

(B) Starting on a separate sheet, amendments to the specification by presenting replacement paragraphs marked up to show changes made;

(C) Starting on a separate sheet, a complete listing of all of the claims:

- in ascending order;

- with status identifiers; and

- with markings in the currently amended claims;

(D) Starting on a separate sheet, the Remarks.

It is not believed that extensions of time or fees for net addition of claims are required beyond those that may otherwise be provided for in documents accompanying this paper.

However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefore (including fees for net addition of claims) are hereby authorized to be charged to our Deposit Account No. 19-0036.

Amendments to the Specification

Applicants submit no amendments to the specification.

Amendments to the Claims

The listing of claims will replace all prior versions, and listings of claims in the application.

Claim 1-5 (cancelled)

Claim 6 (currently amended): A phase locked loop circuit with dual gate dielectric thicknesses, comprising:

an oscillator to output a reference clock signal;

a reference frequency divider to receive and divide the reference clock signal, and output a reference signal;

a comparison frequency divider to receive a control voltage signal and output a comparison signal;

a phase comparator to receive the reference signal and the comparison signal, wherein said phase comparator compares the reference signal with the comparison signal and outputs a frequency difference signal and a phase difference signal;

a charge pump to receive the frequency difference and the phase difference signals and output a charge pump signal;

a low-pass filter to receive the charge pump signal and output a low pass filter signal; and

a voltage controlled oscillator to receive the low pass filter signal and output the control voltage signal,

wherein said oscillator, said reference frequency divider, said comparison frequency divider, said phase comparator, said charge pump, and said voltage controlled oscillator comprise devices having thin gate oxide layers;

wherein said low-pass filter comprises a capacitor formed by

an N-type substrate;

a P-type region within said N-type substrate;

a thick oxide layer formed over said P-type region;

a P^+ gate electrode formed over said thick oxide layer and coupled to a first voltage supply line; and

P^+ pick-up terminals within said P-type region adjacent ~~the~~ said gate electrode and coupled to a second voltage supply line; and

wherein said thick oxide layer of said capacitor reduces leakage current such that a gate-to-substrate voltage of said capacitor is maintained, thereby maintaining a stable control voltage for the phase locked loop circuit.

Claim 7 (currently amended): The circuit of claim 6, wherein [[a]] the gate-to-substrate voltage of said capacitor is maintained at less than zero volts.

Claim 8 (original): The circuit of claim 6, wherein said P^+ gate comprises polysilicon.

Claim 9 (original): The circuit of claim 6, wherein said N-type substrate comprises a deep NWELL.

Claim 10 (currently amended): The circuit of claim 6, wherein said thick oxide layer is between about 20 and 100 Å thick.

Claim 11 (currently amended): In a low-pass filter for a phase locked loop (PLL) circuit with dual gate dielectric thicknesses, wherein the PLL circuit additionally includes an oscillator, a reference frequency divider, a comparison frequency divider, a phase comparator, a charge pump, and a voltage controlled oscillator each comprising devices having thin gate oxide layers, a capacitor comprising:

an N-type substrate;

a P-type region within said N-type substrate;

a thick oxide layer formed over said P-type region;

a P^+ gate electrode formed over said thick oxide layer and coupled to a first voltage supply line; and

P^+ pick-up terminals within said P-type region adjacent ~~the~~ said gate electrode and coupled to a second voltage supply line,

wherein said thick oxide layer of the capacitor reduces leakage current whereby a gate-to-substrate voltage of the capacitor is maintained at less than zero volts to maintain a stable control voltage for the PLL circuit.

Claim 12 (cancelled)

Claim 13 (original): The capacitor of claim 11, wherein said P^+ gate electrode comprises polysilicon.

Claim 14 (original): The capacitor of claim 11, wherein said N-type substrate comprises a deep NWELL.

Claim 15 (currently amended): The capacitor of claim 11, wherein said thick oxide layer is between about 20 and 100 Å thick.

Claim 16-24 (cancelled)

Claim 25 (new): A phase locked loop circuit with dual gate dielectric thicknesses, comprising:

an oscillator to output a reference clock signal;

a reference frequency divider to receive and divide the reference clock signal, and output a reference signal;

a comparison frequency divider to receive a control voltage signal and output a comparison signal;

a phase comparator to receive the reference signal and the comparison signal, wherein said phase comparator compares the reference signal with the comparison signal and outputs a frequency difference signal and a phase difference signal;

a charge pump to receive the frequency difference and the phase difference signals and output a charge pump signal;

a low-pass filter to receive the charge pump signal and output a low pass filter signal; and

a voltage controlled oscillator to receive the low pass filter signal and output the control voltage signal,

wherein said oscillator, said reference frequency divider, said comparison frequency divider, said phase comparator, said charge pump, and said voltage controlled oscillator comprise devices having thin gate oxide layers;

wherein said low-pass filter includes a capacitor that comprises at least one device having a thick gate oxide layer; and

wherein said thick gate oxide layer of said capacitor reduces leakage current such that a gate-to-substrate voltage of said capacitor is maintained, thereby maintaining a stable control voltage for the phase locked loop circuit.

COPY AS FILED

Remarks

Upon entry of the foregoing amendment, claims 6-11, 13-15, and 25 are pending in the application, with claims 6, 11, and 25 being the independent claims. Claims 1-5, 12, and 16-24 are sought to be cancelled without prejudice to or disclaimer of the subject matter therein. New claim 25 is sought to be added. Independent claims 6 and 11 are amended for further clarification. Claims 7, 10, and 15 are amended for purposes of clarity in light of the amendment to independent claims 6 and 11. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Based on the above amendment and the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Rejections under 35 U.S.C. § 102

The Office Action states on page 2 that claims 1-3, 16-17, and 20-22 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Pat. No. 6,621,128 B2 to Lee *et al.* (hereinafter, "Lee"). In an effort to expedite prosecution of this application, claims 1-5, 12, and 16-24, which include the rejected claims, have been cancelled by amendment without prejudice to or disclaimer of the subject matter therein. Therefore, the rejection of these claims is now moot.

Rejections under 35 U.S.C. § 103

The Office Action states on page 3 that claims 4-5, 18-19, and 23-24 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee in view of U.S. Pat. No. 6,303,957

B1 to Ohwa (hereinafter, "Ohwa"). As stated above, these claims have been cancelled by amendment. Therefore, the rejection of these claims is now moot.

The Office Action states on page 4 that claims 6-8 and 11-13 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee in view of "Applicant admitted prior art" and U.S. Pat. No. 4,335,359 to Kriedt *et al.* (hereinafter, "Kriedt"). Based on the above amendment and the following remarks, Applicants respectfully request that the Examiner reconsider the rejection of these claims.

The cited art, either alone or in combination, does not teach or suggest a phase locked loop (PLL) circuit with dual gate dielectric thicknesses in which the PLL components including "*said oscillator, said reference frequency divider, said comparison frequency divider, said phase comparator, said charge pump, and said voltage controlled oscillator comprise devices having thin gate oxide layers*," while the low-pass filter of the PLL comprises a capacitor which includes a *thick gate oxide layer*, as claimed in amended independent claim 1, for example. (Support for this is found in paragraphs 27 and 29 of the specification, for example.) Independent claim 11 and new independent claim 25 are similarly directed toward a phase locked loop circuit with dual gate dielectric thicknesses. The technical significance of this is that having a thick oxide layer in the capacitor of the low pass filter reduces leakage current that can be severe in the otherwise thin oxide phase locked loop circuit. The reduction in leakage current allows a stable control voltage to be maintained for the phase locked loop circuit. (See paragraph 9 of the specification for a discussion of the problem being solved.) For at least this reason, independent claims 6 and 11 and the claims depending therefrom, as well as new independent claim 25, are believed to

be allowable. Therefore, Applicants respectfully request that the Examiner reconsider the rejections of these claims and that they be withdrawn.

On page 5, the Office Action states that claims 9-10 and 14-15 are rejected under U.S.C. § 103(a) as being unpatentable over Lee in view of "Applicant admitted prior art" and Kriedt, and further in view of Ohwa. These claims depend directly from either independent claim 6 or 11. Thus, dependent claims 9-10 and 14-15 are believed to be allowable for at least the same reason as discussed above for independent claims 6 and 11. Therefore, Applicants respectfully request that the Examiner reconsider the rejections of these claims and that they be withdrawn.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Donald J. Featherstone
Attorney for Applicants
Registration No. 33,876

Date: 6/30/04

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

PTO/SB/44 (04-04)
Approved for use through 04/30/2007. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.
(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,828,654 B2

DATED : December 7, 2004

INVENTOR(S) : Derek Tam et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Claim 1, column 6, line 55, "the said gate electrode and coupled to a second" should appear as --said gate electrode and coupled to a second--.

Claim 2, column 6, line 61, "The circuit of claim 1, wherein said P+ gate-to-substrate" should appear as --The circuit of claim 1, wherein the gate-to-substrate--.

Claim 6, column 7, line 5, "circuit additionally includes oscillator, a reference frequency" should appear as --circuit additionally includes an oscillator, a reference frequency--.

MAILING ADDRESS OF SENDER:

Sterne, Kessler, Goldstein & Fox P.L.L.C.
1100 New York Avenue, N.W.
Washington, DC 20005-3934

PATENT NO. 6,828,654 B2

No. of additional copies